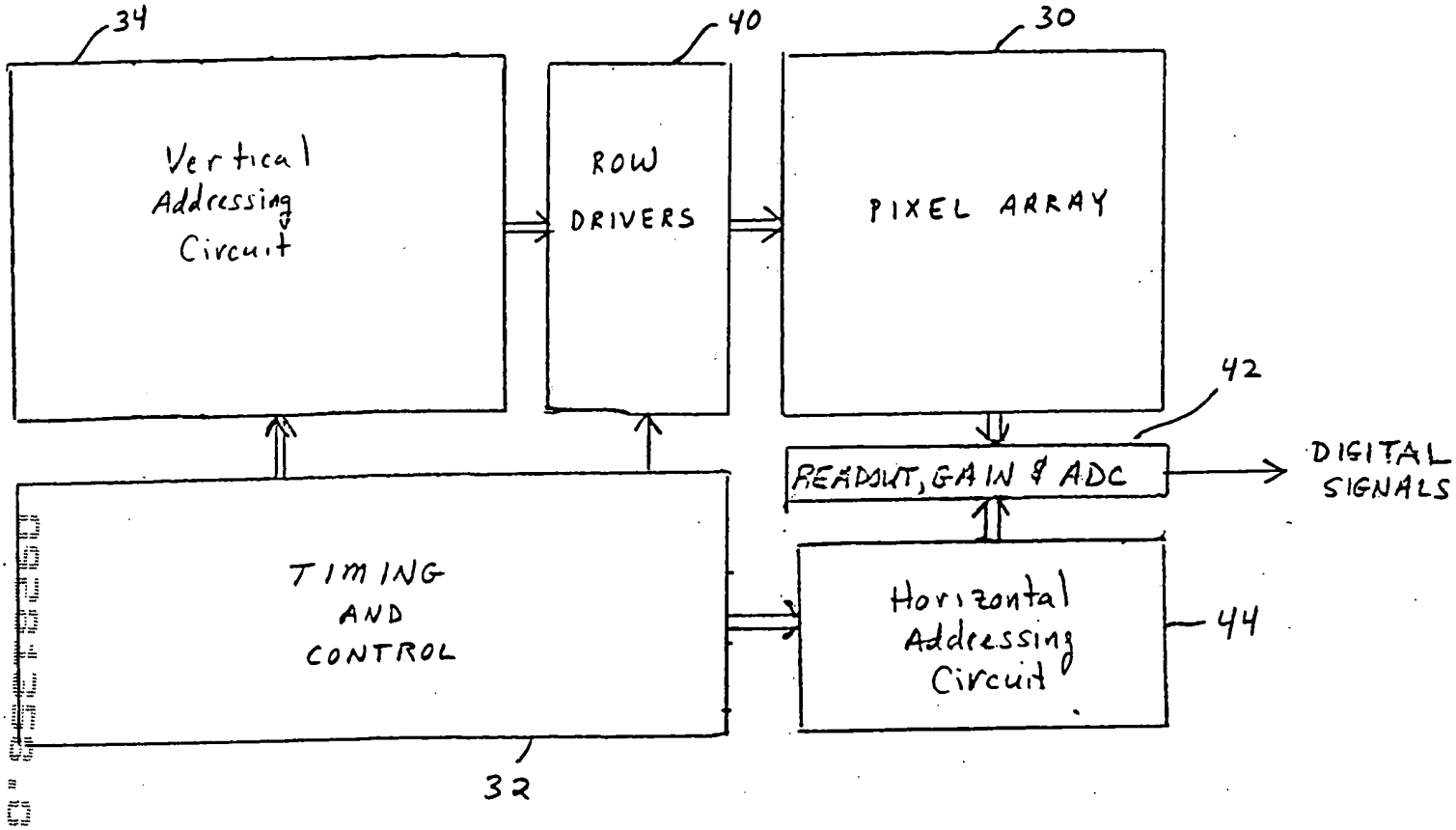

34
40
30
Vertical Addressing Circuit
ROW DRIVERS
PIXEL ARRAY
42
READOUT, GAIN & ADC
DIGITAL SIGNALS
TIMING AND CONTROL
Horizontal Addressing Circuit
44
32

FIG. 1

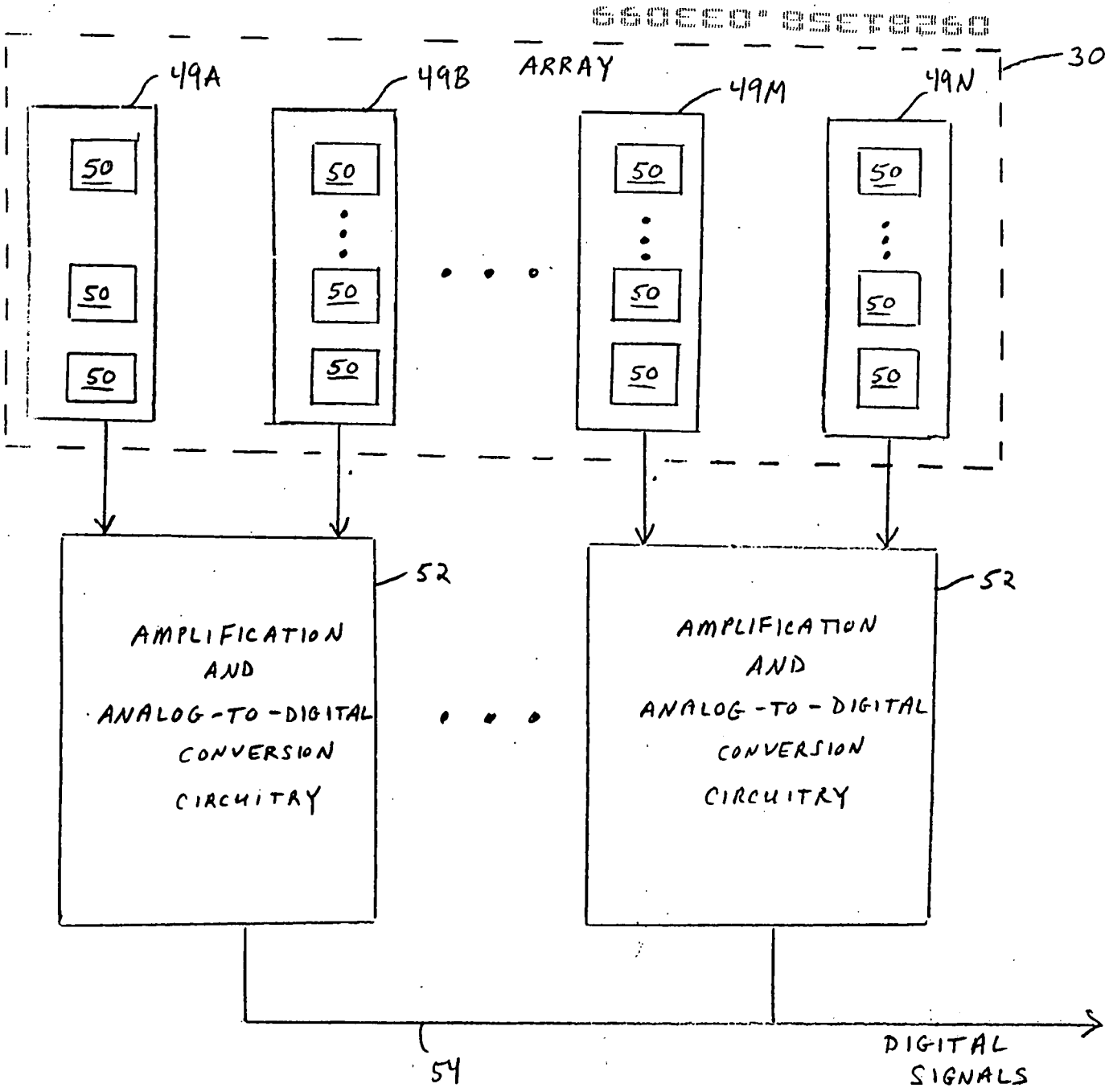

ARRAY
30
49A
49B
49M
49N
50
52
AMPLIFICATION AND ANALOG-TO-DIGITAL CONVERSION CIRCUITRY
54
DIGITAL SIGNALS

FIG. 2

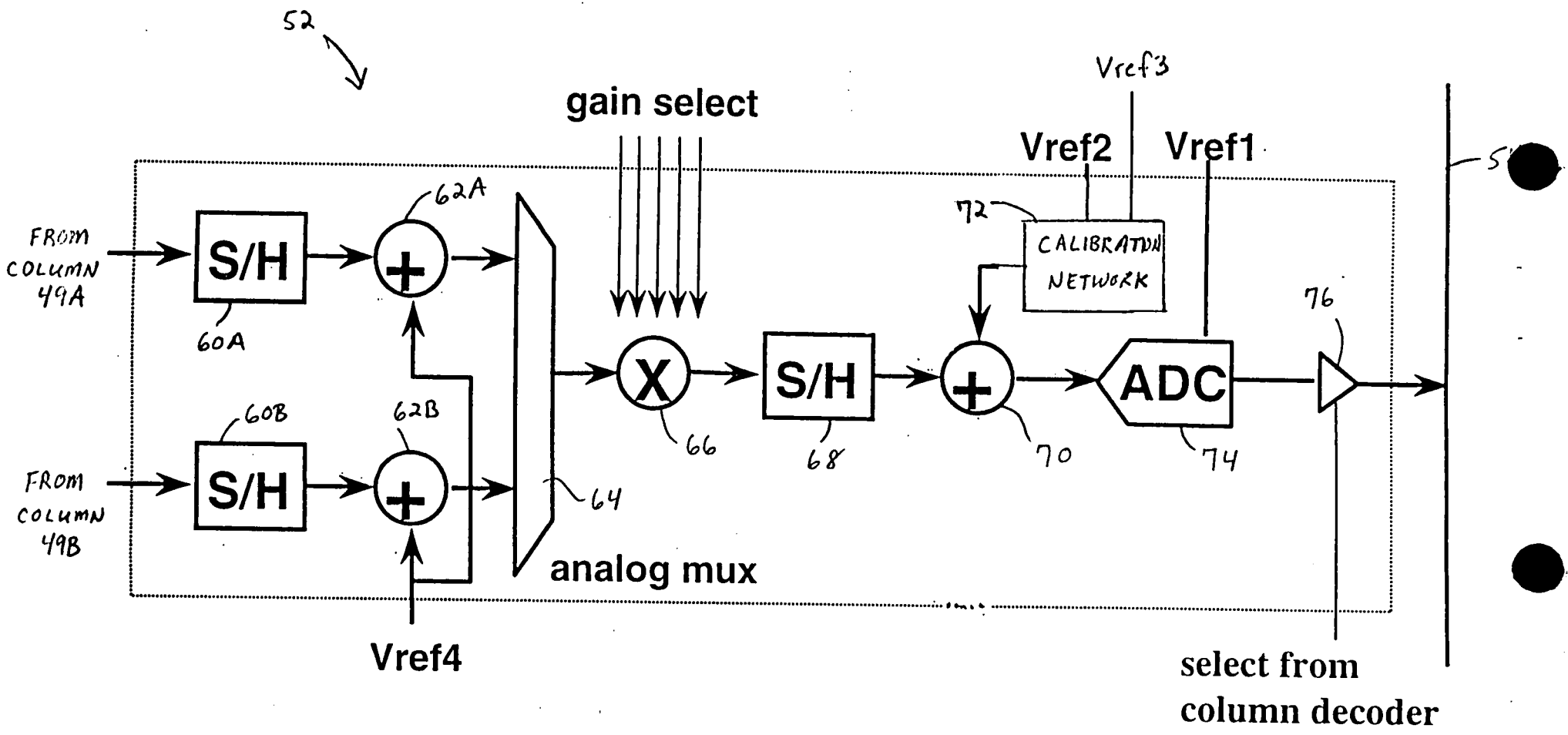

52
gain select
Vref3
Vref2
Vref1
FROM COLUMN 49A
FROM COLUMN 49B
S/H
60A
60B
62A
62B
72
CALIBRATION NETWORK
X
66
S/H
68
70
ADC
74
76
64
analog mux
Vref4
select from column decoder

FIG. 3

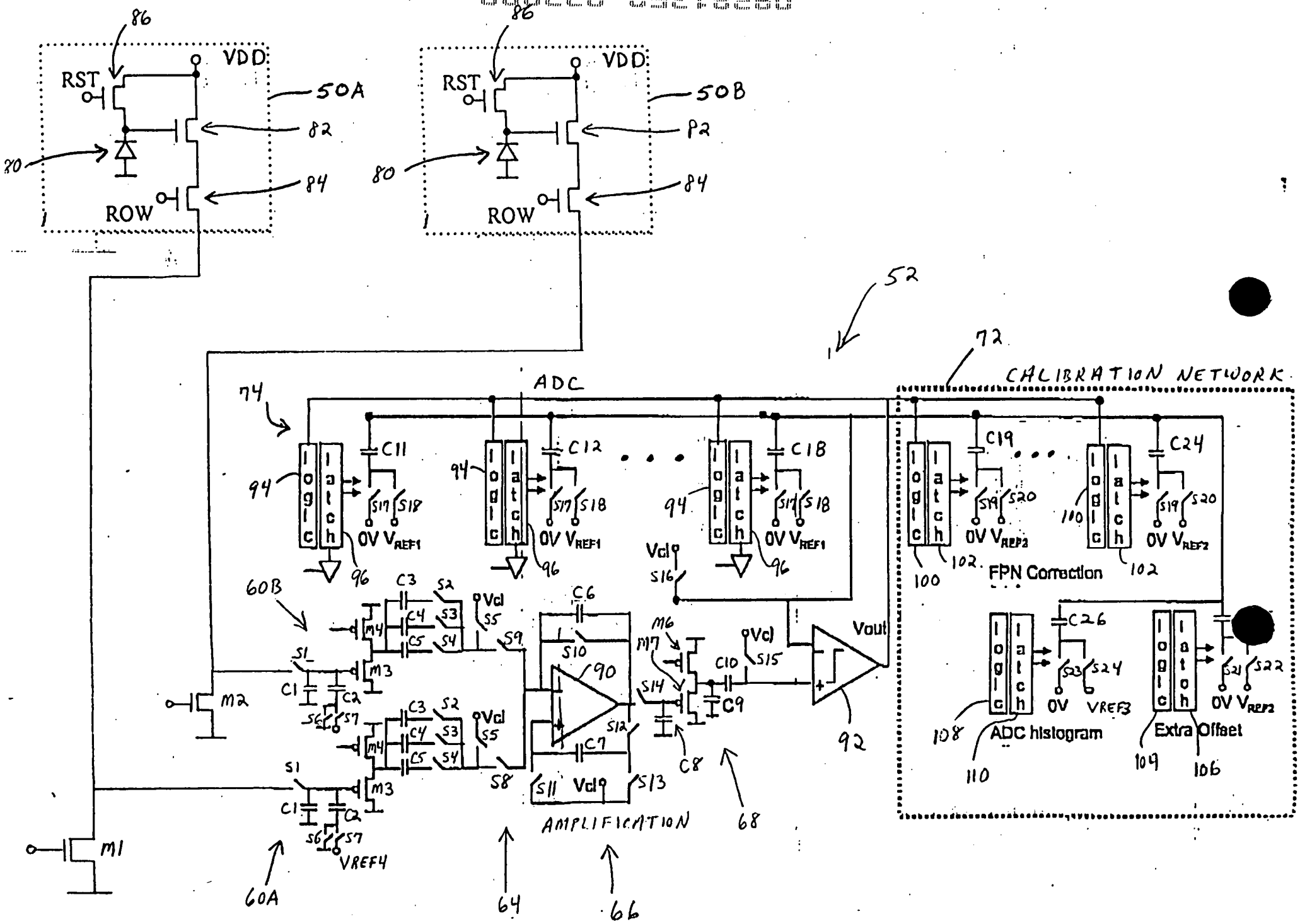
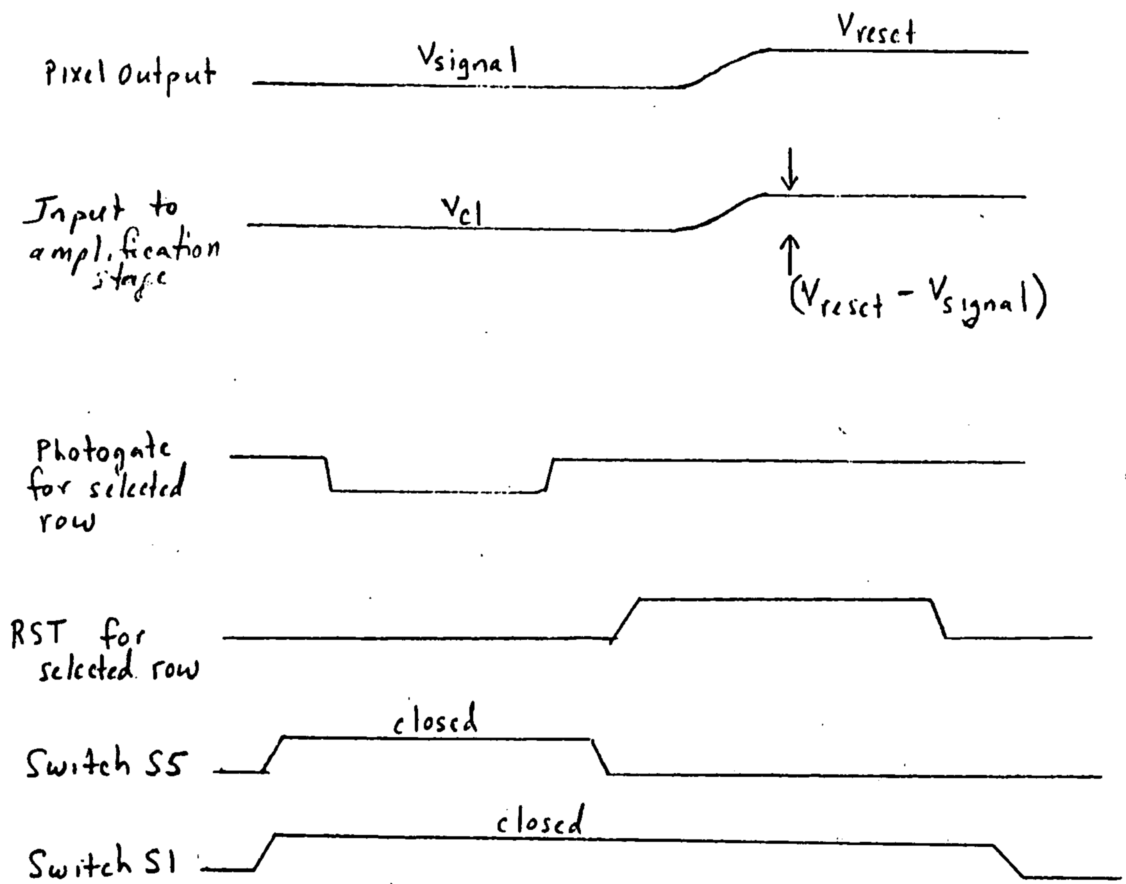

86
VDD
RST
50A
82
80
84
ROW
86
VDD
RST
50B
P2
80
84
ROW
52
72
CALIBRATION NETWORK
74
ADC
94
C11
C12
C18
S17
S18
0V
VREF1
96
C19
C24
S19
S20
VREF2
110
100
102
FPN Correction
60B
C3
S2
C4
S3
C5
S4
Vcl
S5
S9
M4
M3
S1
C1
C2
S6
S7
M2
C6
S10
90
M6
M7
S14
C10
S15
Vout
92
C9
C8
S12
C7
S11
S13
AMPLIFICATION
68
C26
S23
S24
VREF3
ADC histogram
108
Extra Offset
109
106
S21
S22
M1
VREF4
60A
64
66

FIG. 4



SAMPLE AND HOLD TIMING

FIG. 5

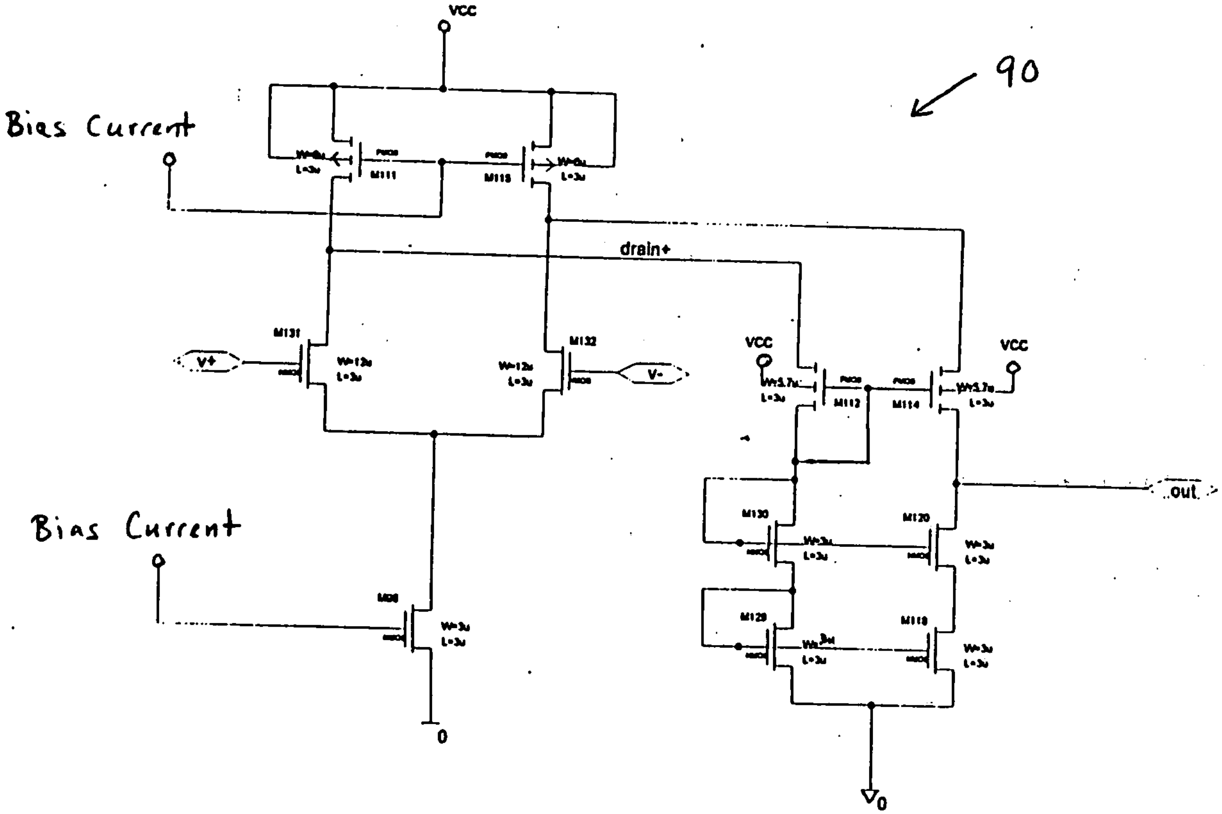
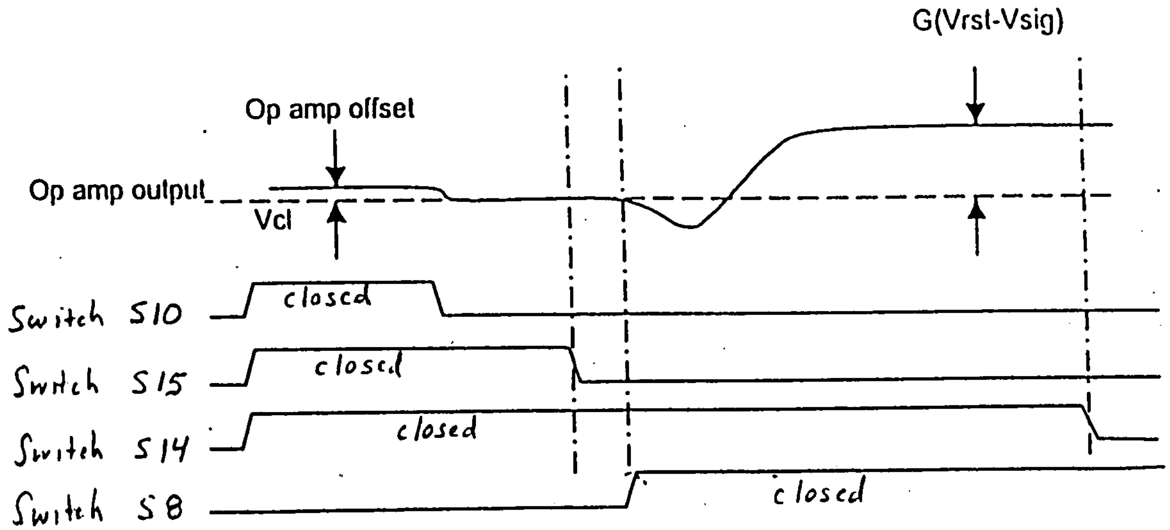


FIG. 6



Amplification Timing

FIG. 7

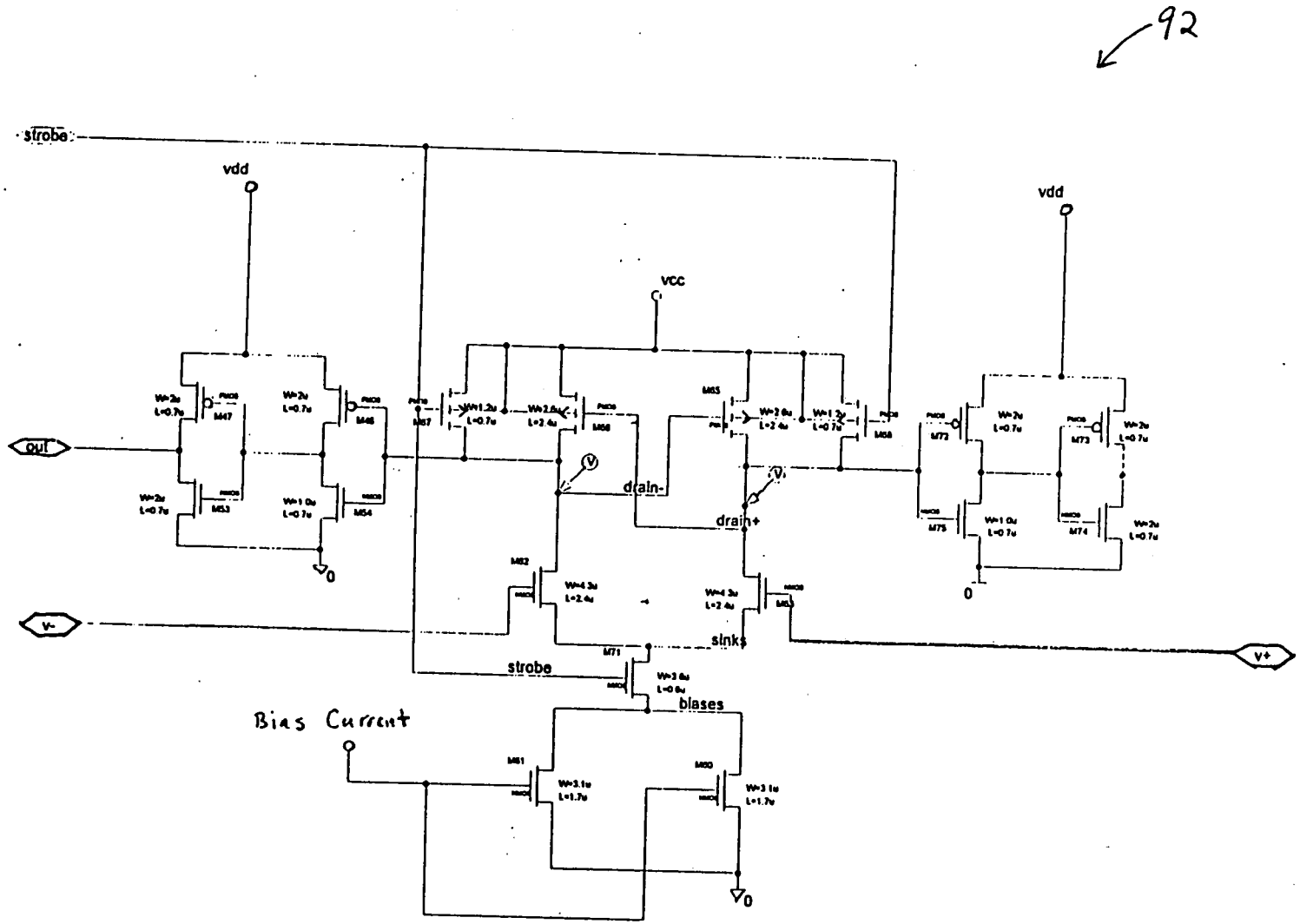

92
strobe
vdd
vdd
vcc
out
drain-
drain+
V-
V+
sinks
strobe
biases
Bias Current
0
0
0

FIG. 8

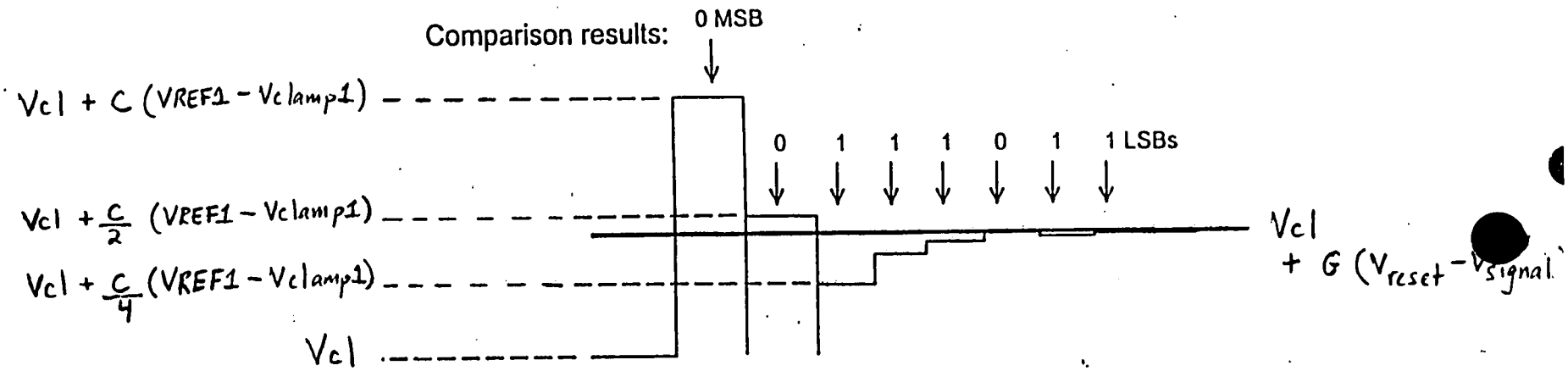


FIG. 9

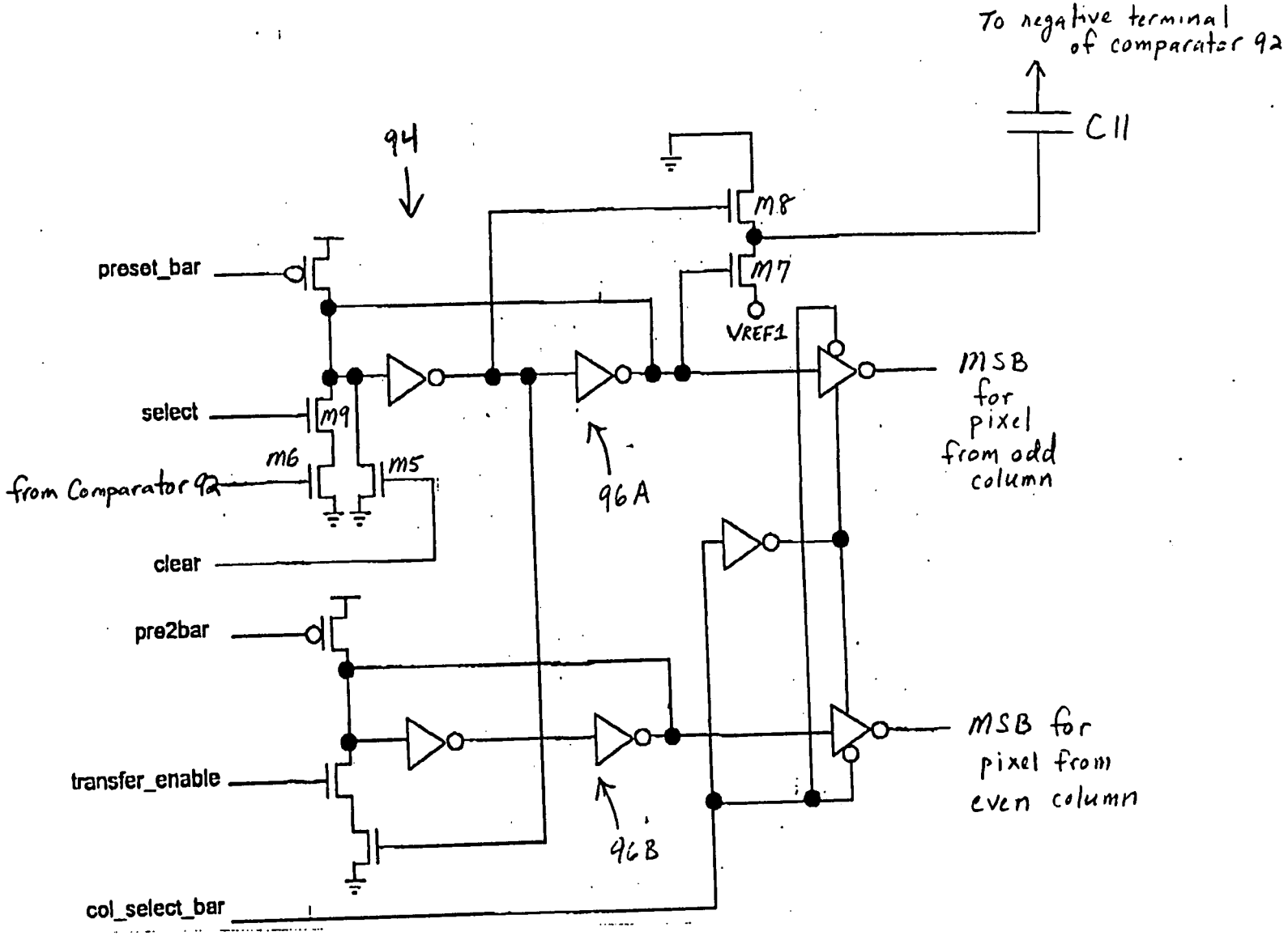

To negative terminal of comparator 92
C11
94
M8
M7
VREF1
preset_bar
select
M9
M6
M5
from Comparator 92
clear
96A
MSB for pixel from odd column
pre2bar
transfer_enable
96B
MSB for pixel from even column
col_select_bar

FIG. 10

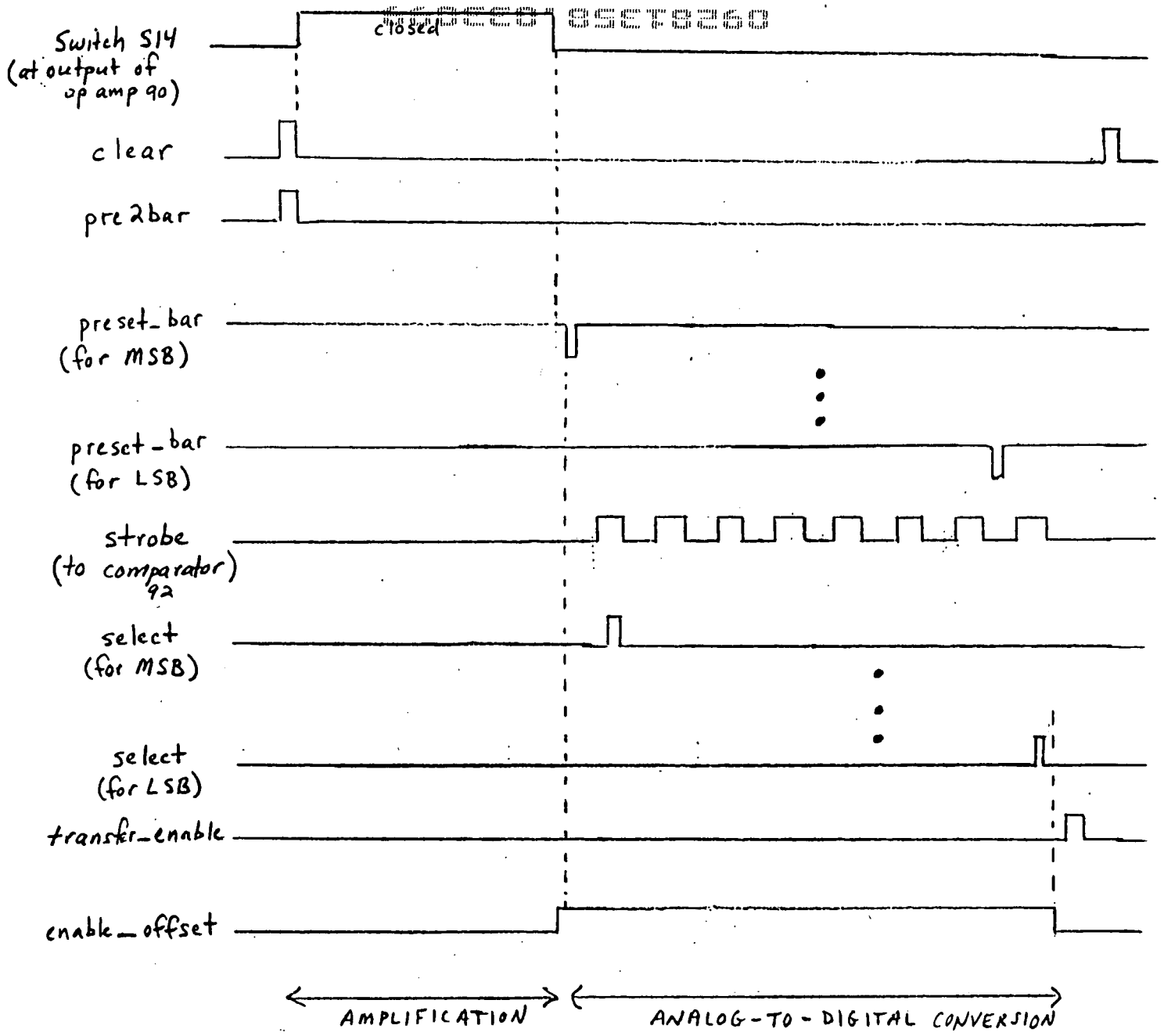

Switch S14
(at output of
op amp 90)
closed
clear
pre2bar
preset_bar
(for MSB)
preset_bar
(for LSB)
strobe
(to comparator
92)
select
(for MSB)
select
(for LSB)
transfer_enable
enable_offset
AMPLIFICATION
ANALOG-TO-DIGITAL CONVERSION

FIG. 11

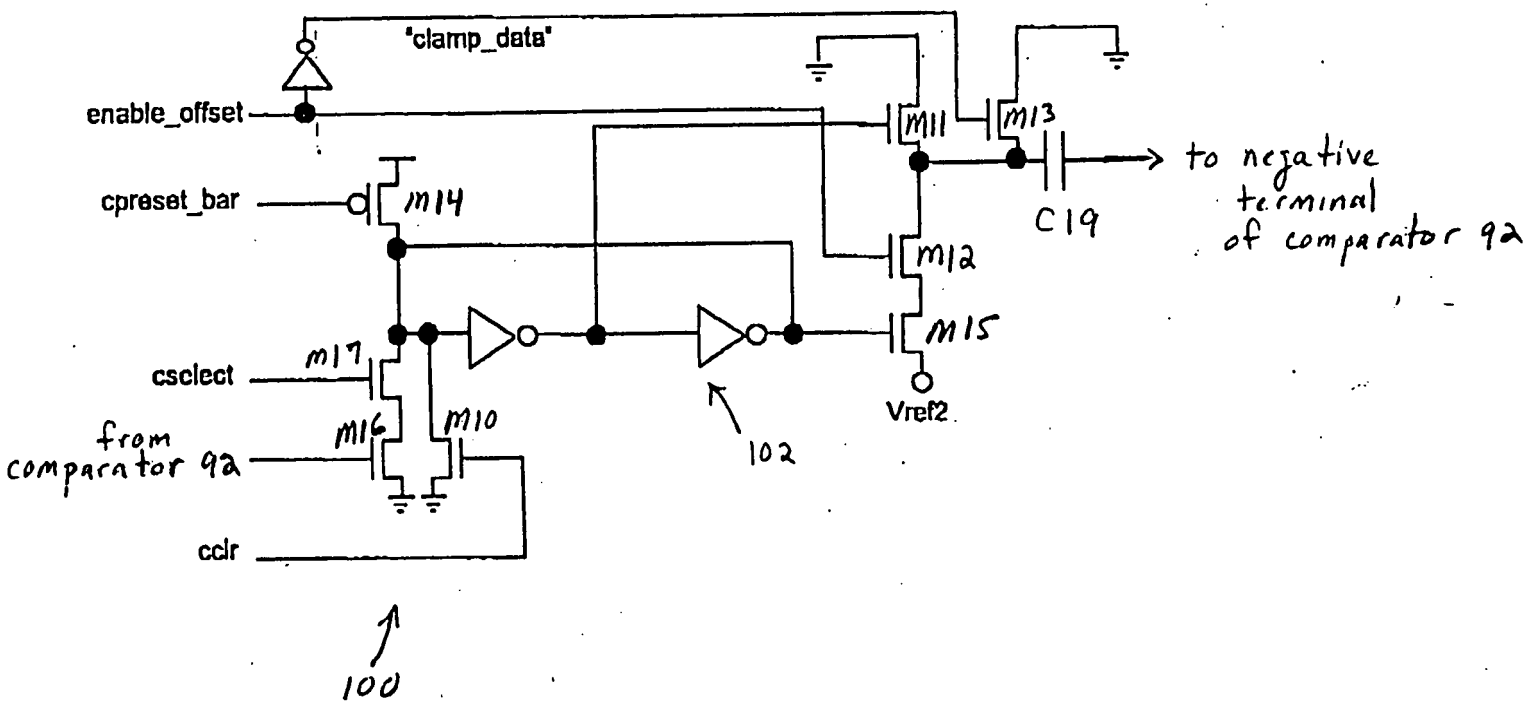
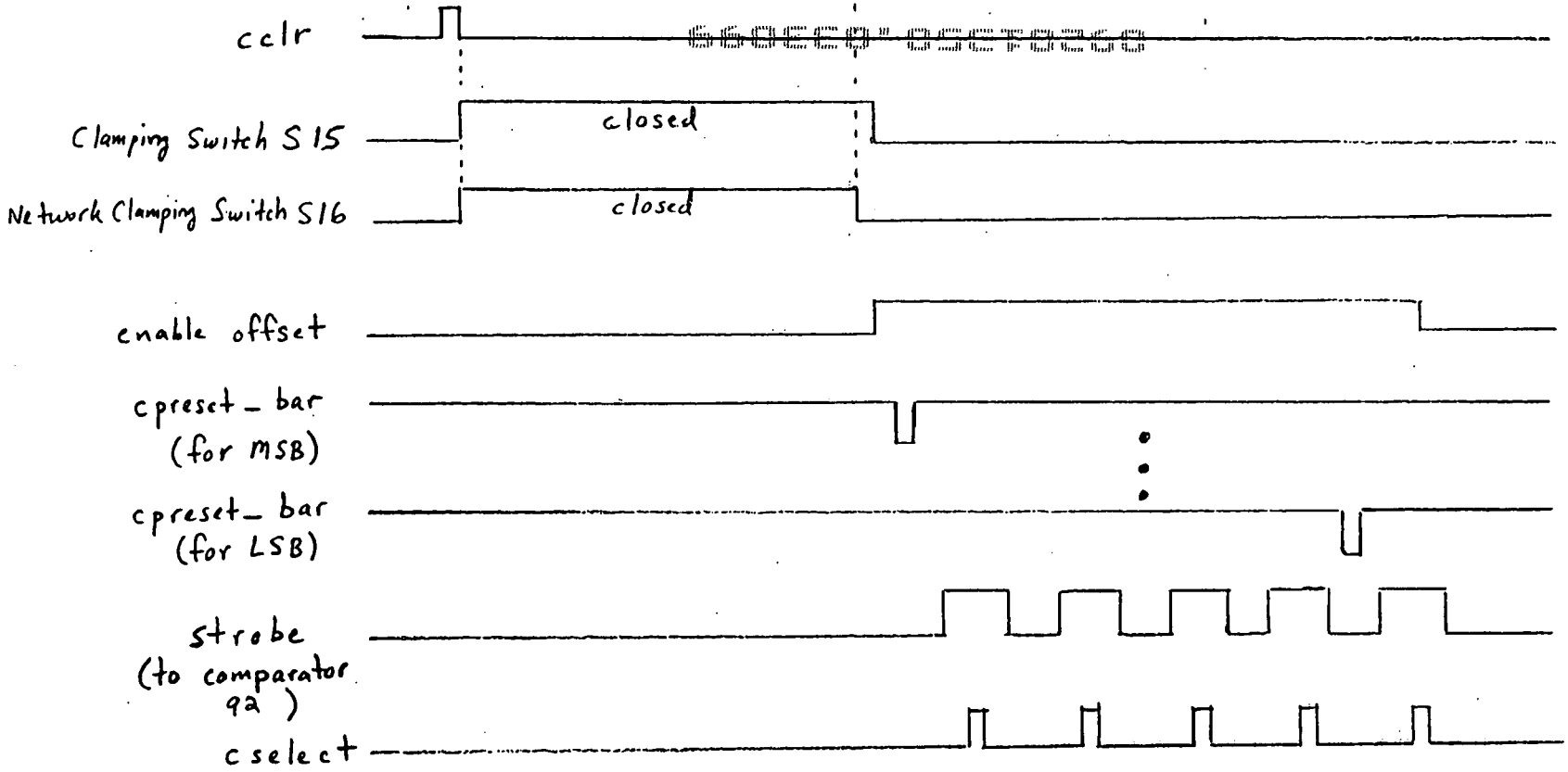

"clamp_data"
enable_offset
cpreset_bar
csclect
from comparator 92
cclr
m14
m17
m16
m10
m11
m13
m12
m15
Vref2
C19
to negative terminal of comparator 92
102
100

FIG. 12



CALIBRATION TIMING

FIG. 13

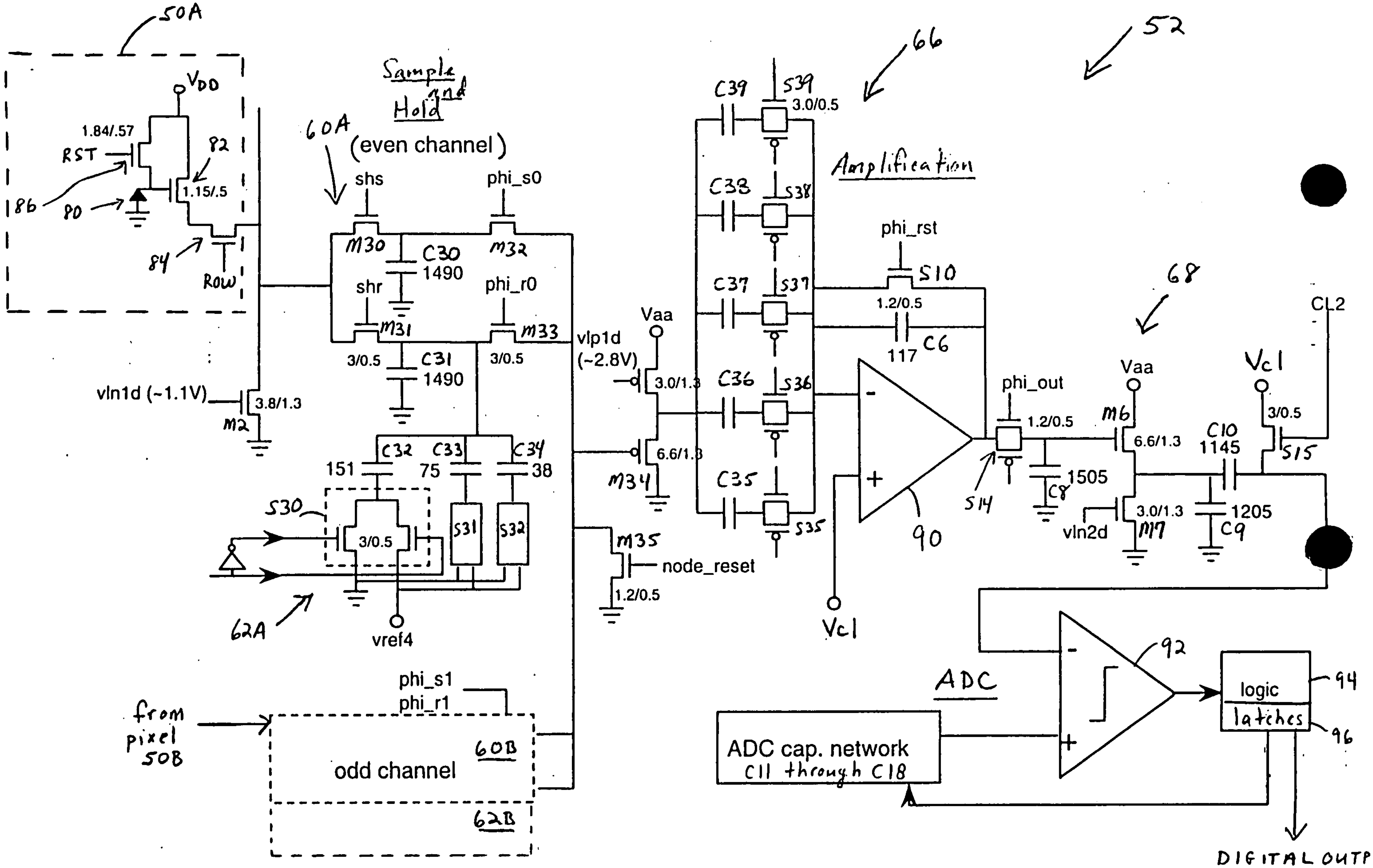

50A
VDD
1.84/.57
RST
86
80
82
1.15/.5
84
ROW
vln1d (~1.1V)
3.8/1.3
M2
Sample and Hold
60A
(even channel)
shs
M30
C30
1490
shr
M31
3/0.5
C31
1490
phi_s0
M32
phi_r0
M33
3/0.5
C32
151
C33
75
C34
38
S30
3/0.5
S31
S32
vref4
62A
vlp1d
(~2.8V)
Vaa
3.0/1.3
6.6/1.3
M34
M35
node_reset
1.2/0.5
from pixel 50B
phi_s1
phi_r1
odd channel
60B
62B
66
C39
S39
3.0/0.5
C38
S38
C37
S37
C36
S36
C35
S35
Amplification
phi_rst
S10
1.2/0.5
117
C6
90
Vcl
52
68
phi_out
1.2/0.5
S14
1505
C8
Vaa
M6
6.6/1.3
3.0/1.3
M7
vln2d
Vcl
3/0.5
S15
CL2
C10
1145
1205
C9
ADC
ADC cap. network
C11 through C18
92
logic
latches
94
96
DIGITAL OUTPUT

FIG. 14

pixel timing

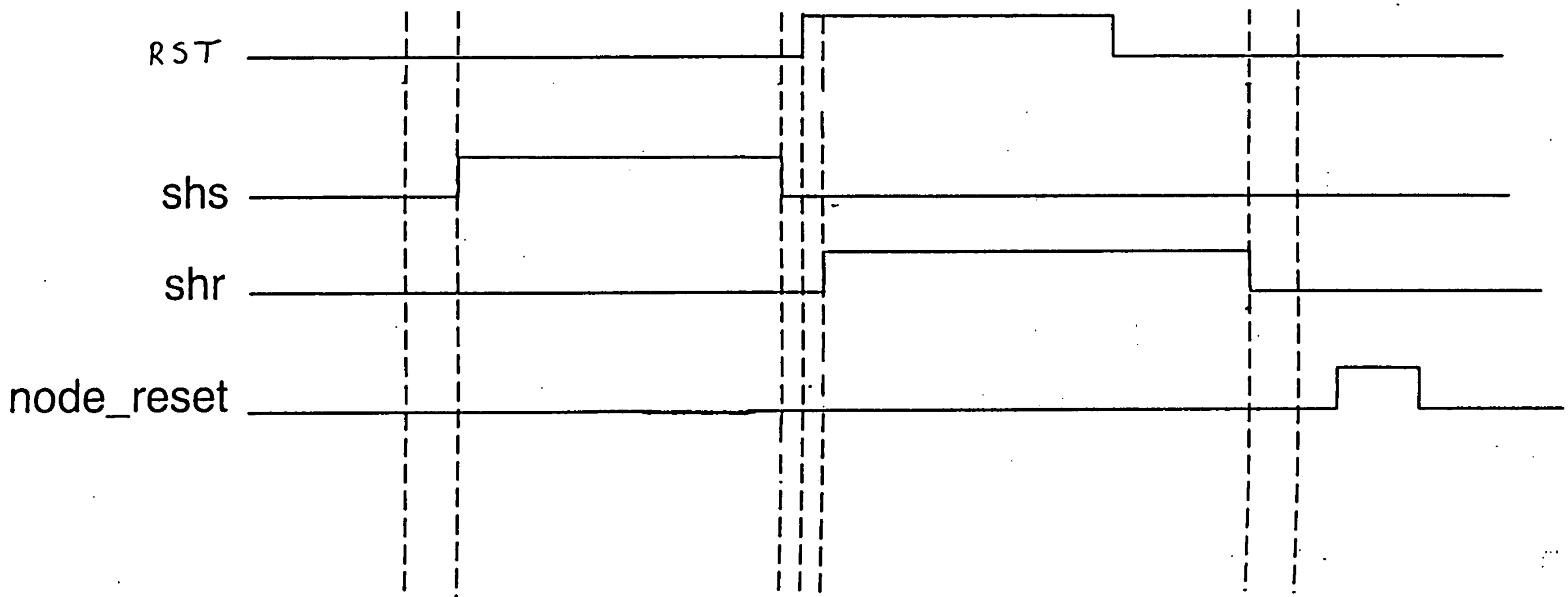


FIG. 15

gain timing

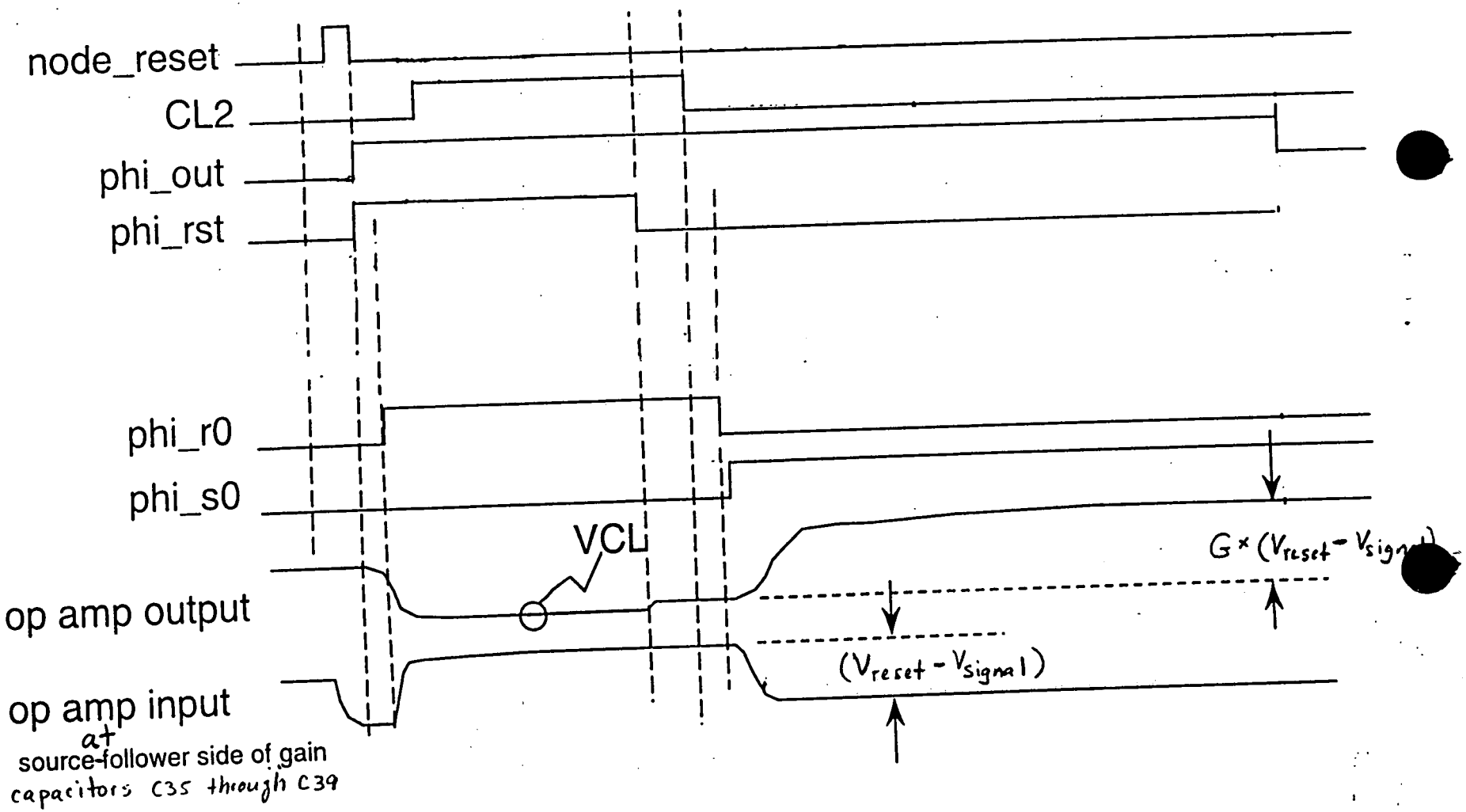


FIG. 16

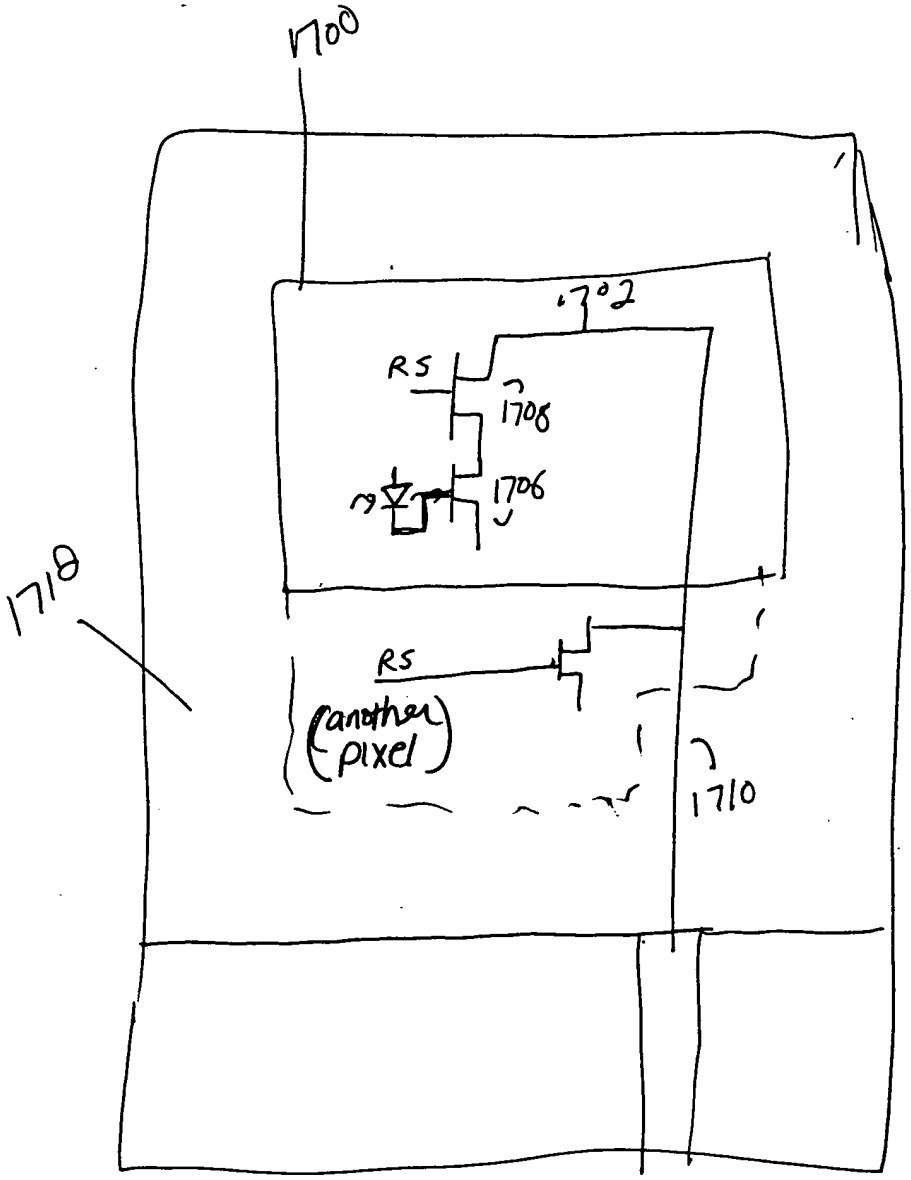


FIG17

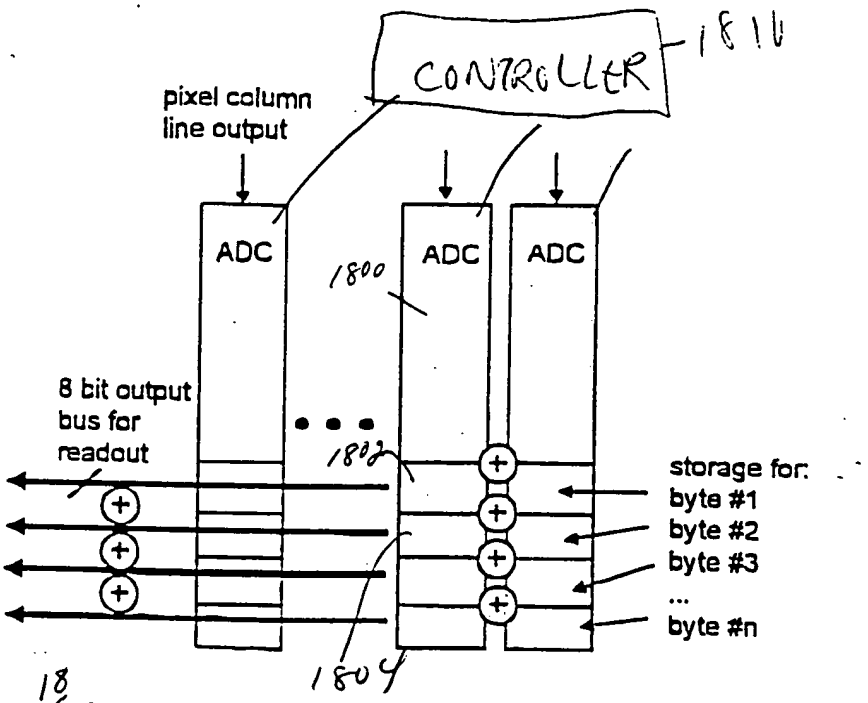


Figure 18. Multiple byte storage inside ADC for column wise multiplexing of the ADC. Arithmetic processing of neighbors also shown.

2 Byte Storage ADC
3/30/98 R. Panicacci